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# H61MX

Fab A

Micro ATX 9.6X8.0

## CPU:

Intel Sandy Bridge processors in LGA1155 Package

## System Chipset:

PCH

## Main Memory:

Dual Channel / DDR-III \* 2 (Max 8GB)

## On Board Device:

PCI Bridge :IT8893E/BX

SIO:IT8728F/CX

LAN:RealTek RTL8111E-VB-GR

HDA Codec:ALC888/ALC662

BIOS:SPI Flash ROM 4M

## Expansion Slots:

PCI EXPRESS 16X SLOT \*1

PCI EXPRESS 1X SLOT \* 1

PCI SLOT \* 2

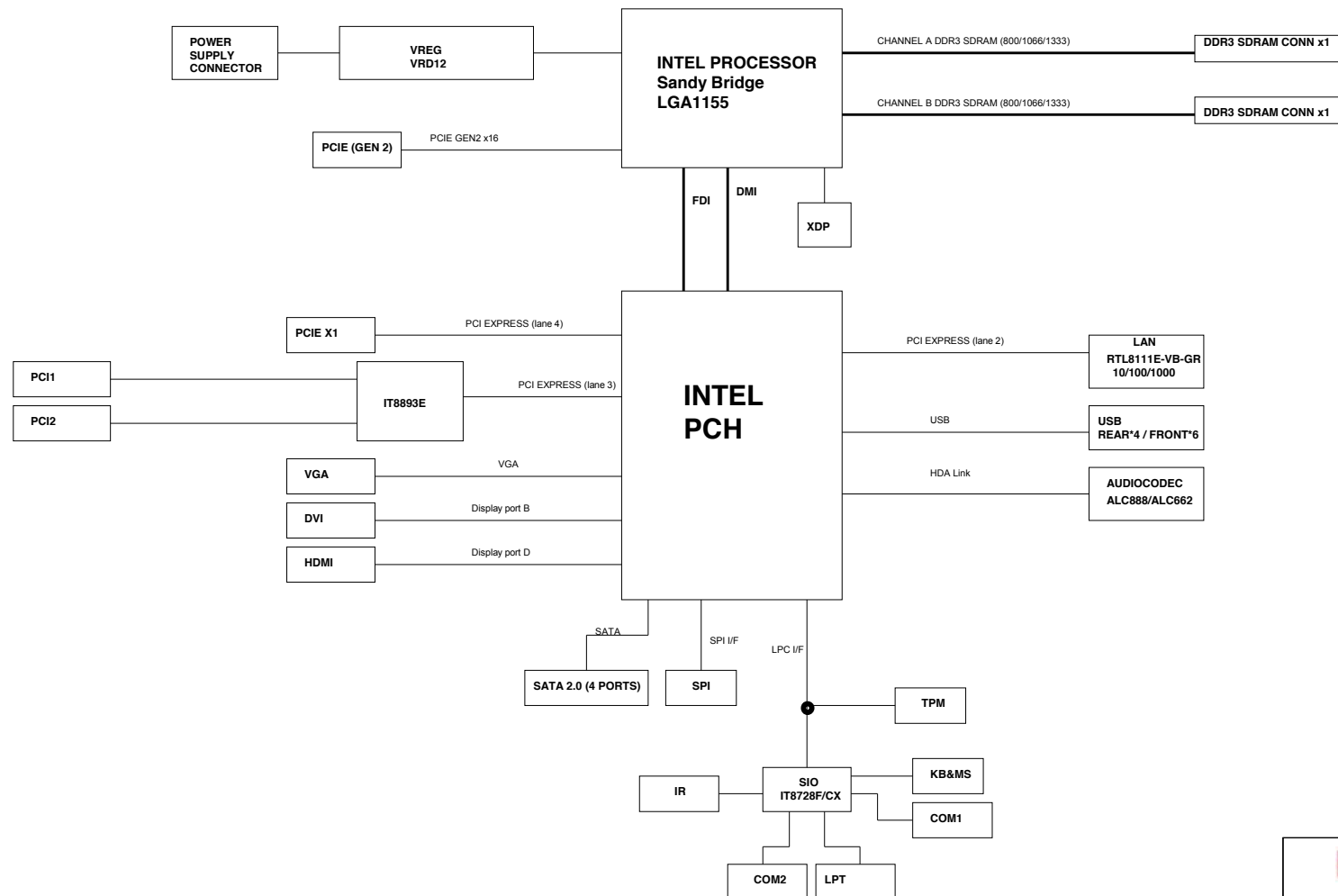
Version	Function	SKU	BOM
Fab.A			



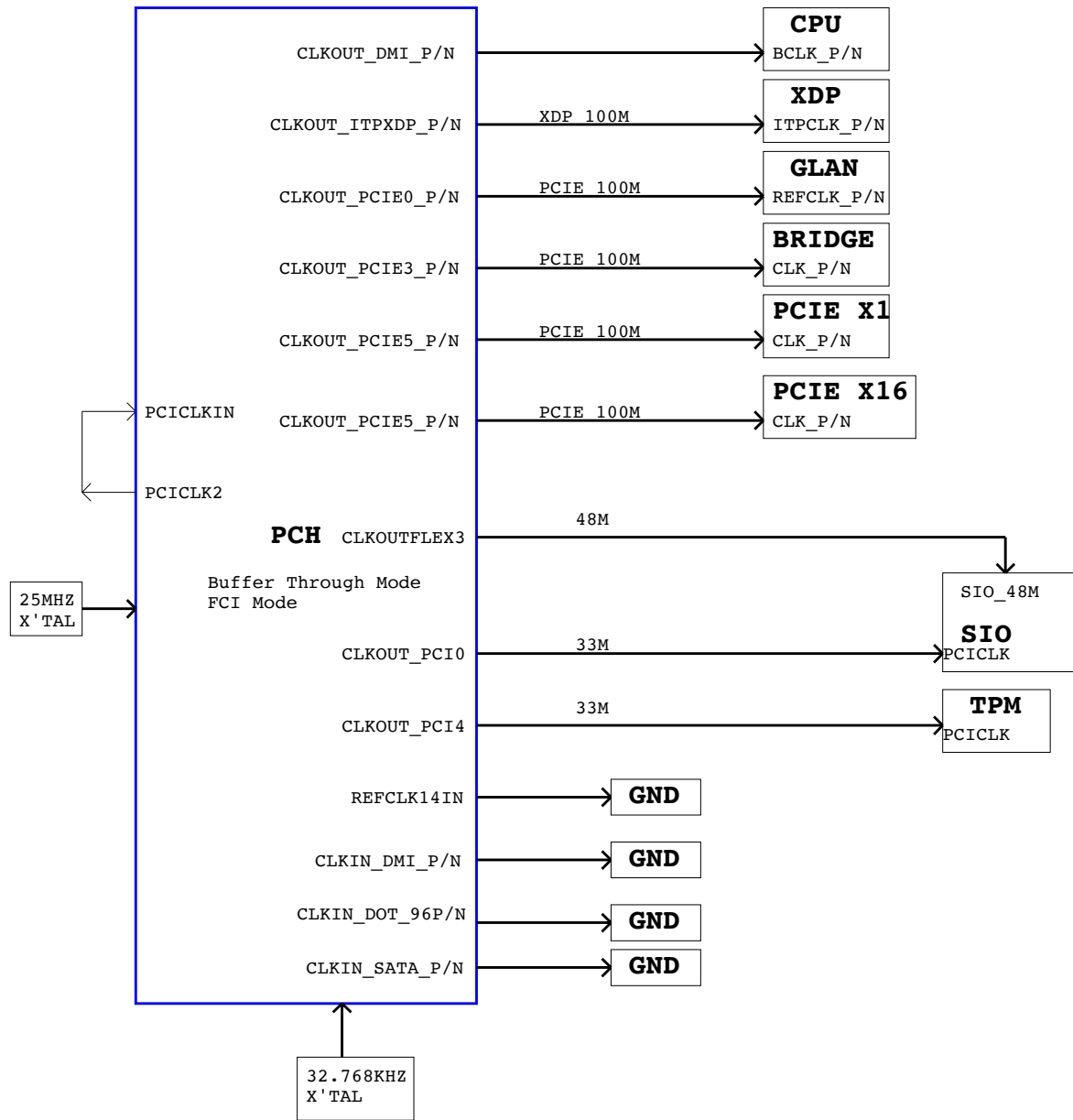
FOXCONN PCEG

Cover Sheet			
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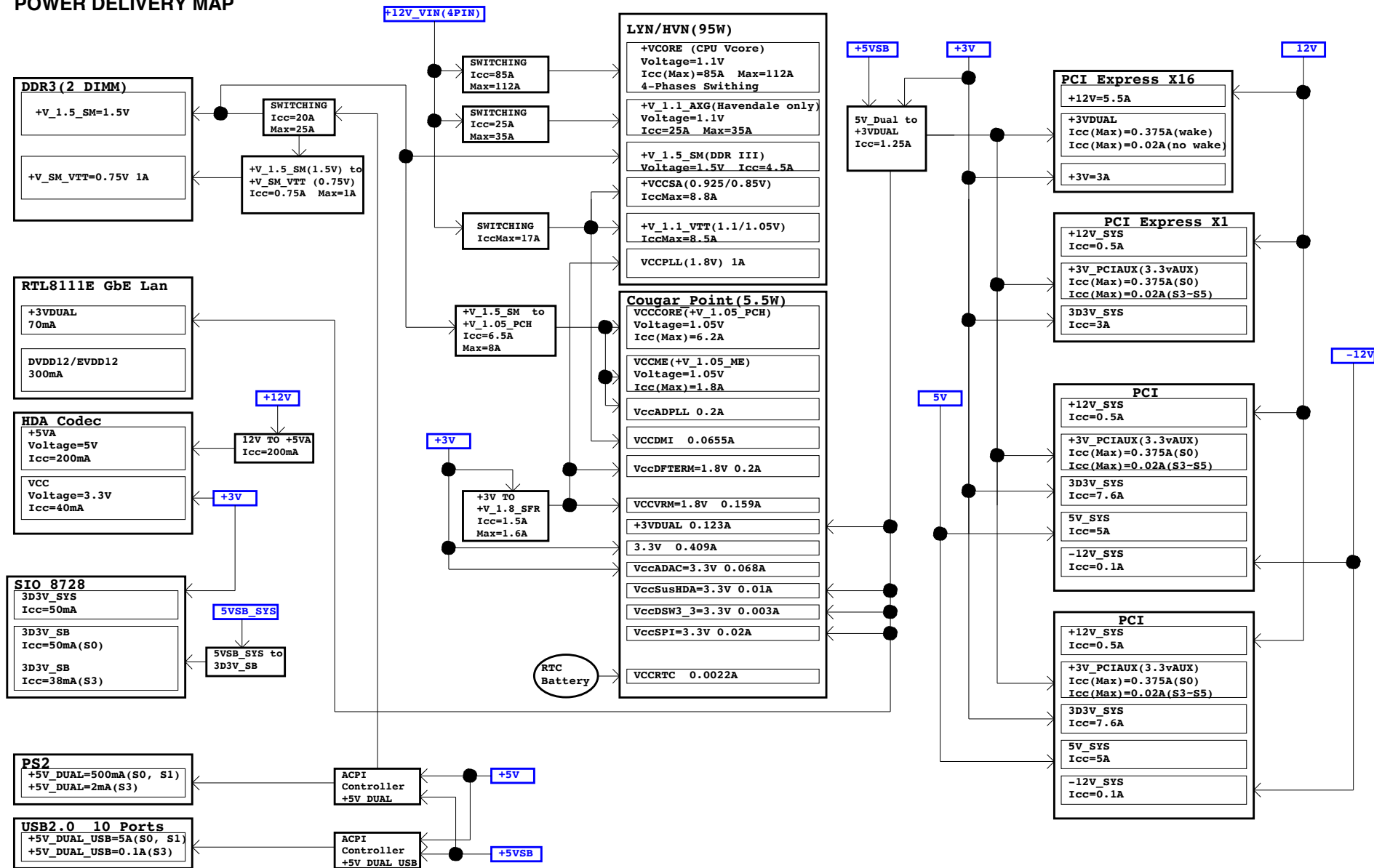
## BLOCK DIAGRAM



# CLOCK DISTRIBUTION



# POWER DELIVERY MAP



[www.vinafix.vn](http://www.vinafix.vn)

<b>FOXCONN</b> FOXCONN PCEG	
File: Power Delivery Map	
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## POWER ON SEQUENCE

### G3 w/RTC Loss to S4/S5 (Without Deep S4/S5 Support) Timing Diagram

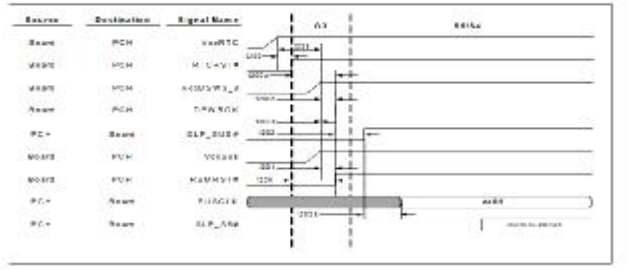


Figure 8-4. S3/M3 to S0 Timing Diagram

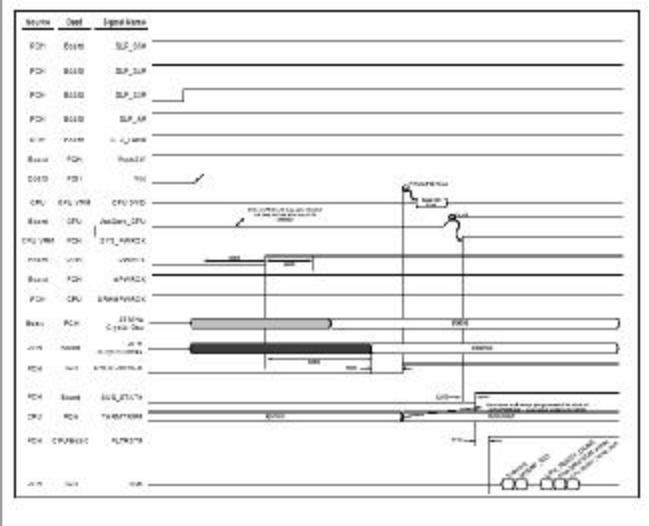


Figure 8-6. DRAMPWROK Timing Diagram

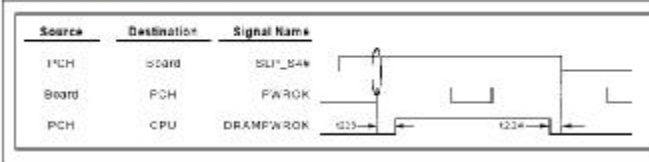


Figure 8-3. S5 to S0 Timing Diagram

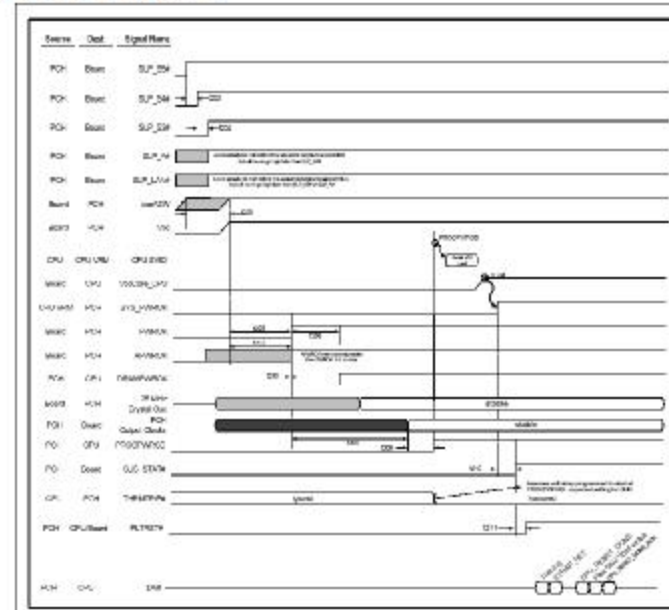
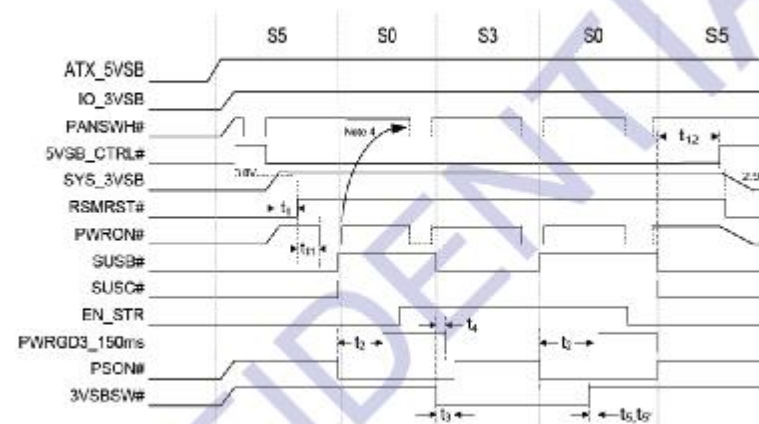


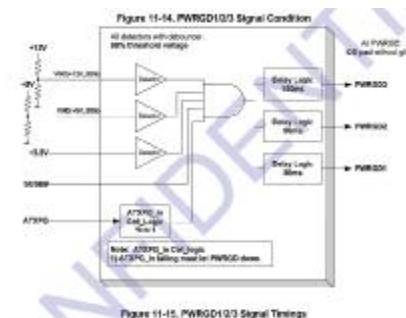
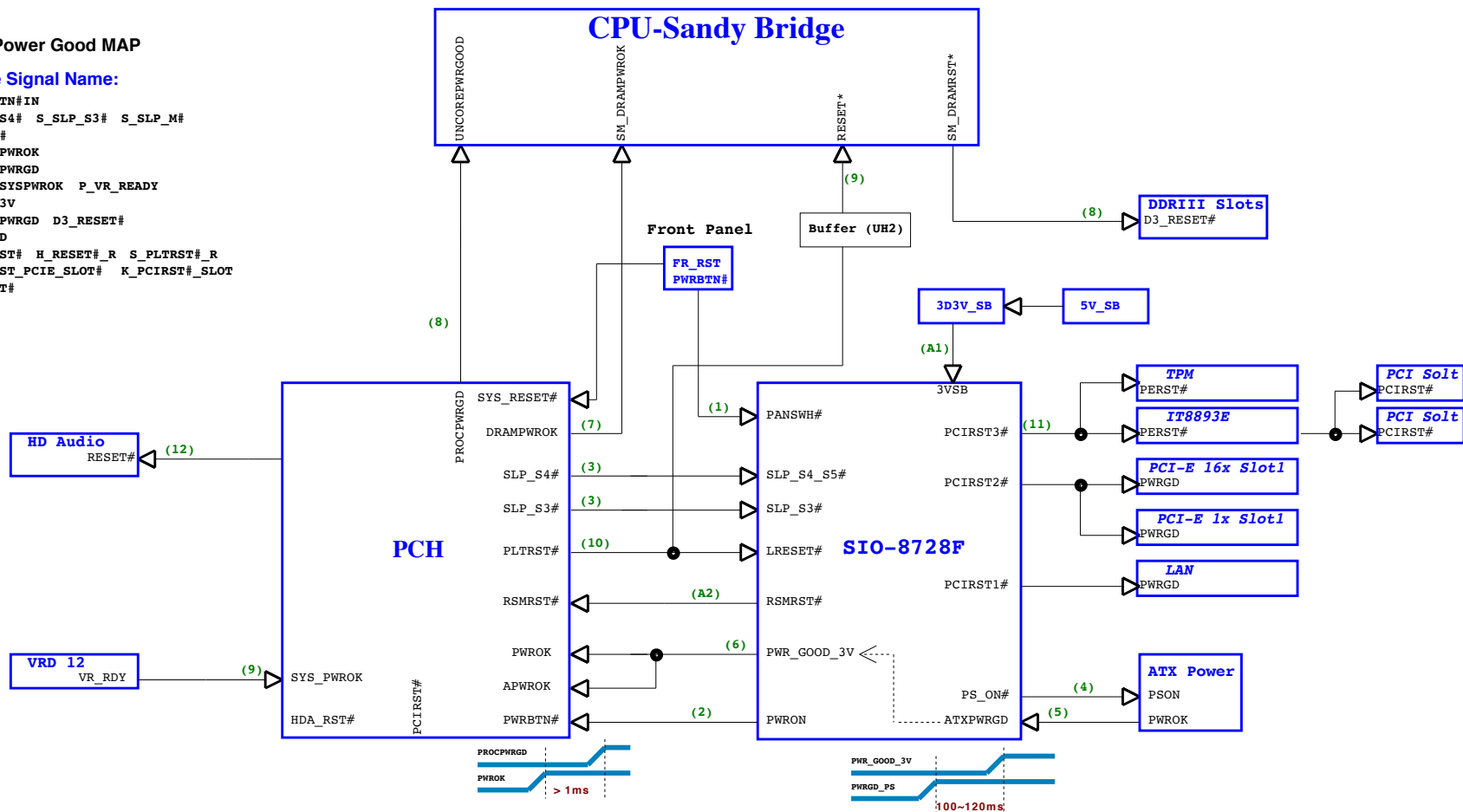
Figure 11-16. EuP Function Signal Timings



# RESET / Power Good MAP

## Sequence Signal Name:

- (1) O\_PWRBTN#IN
- (2) S\_SLP\_S4# S\_SLP\_S3# S\_SLP\_M#
- (3) O\_PSON#
- (4) B\_ATX\_PWROK
- (5) PCH\_MEPWRGD
- (6) S\_PCH\_SYSPWROK P\_VR\_READY
- (7) PWRGD\_3V
- (8) H\_DRAMPWROK D3\_RESET#
- (9) H\_PWRGD
- (10) S\_PLTRST# H\_RESET# R S\_PLTRST# R
- (11) X\_PLTRST# PCIE\_SLOT# K\_PCIRST#\_SLOT
- (12) A\_Z\_RST#



# IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot1	A	B	C	D	16	0	0

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot2	B	C	D	A	17	2	2

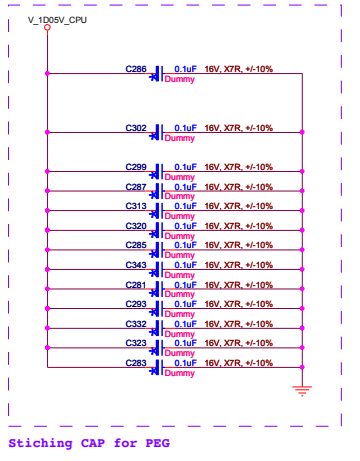
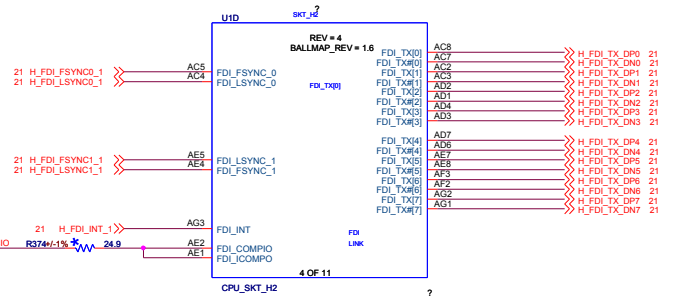
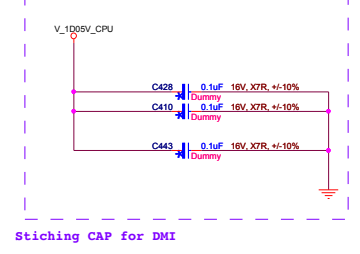
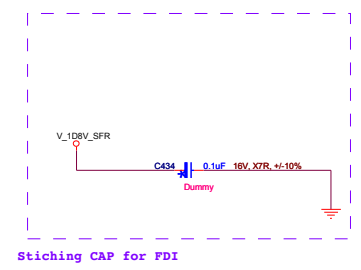
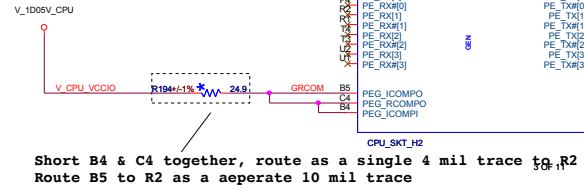
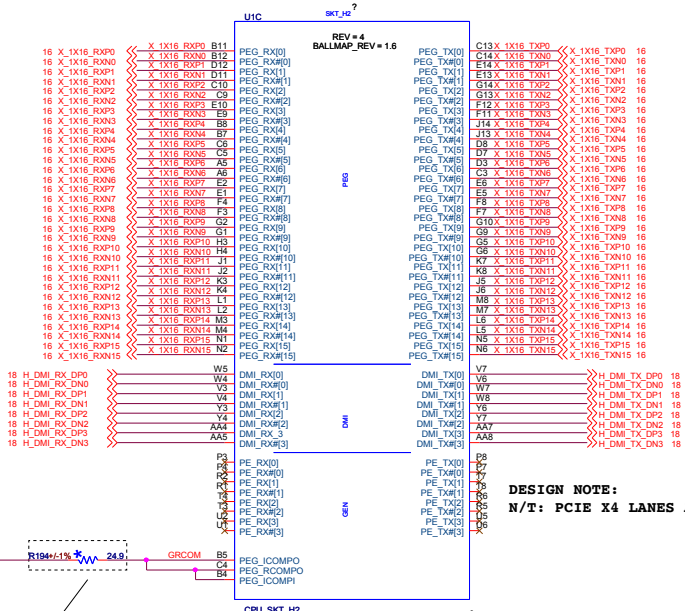
# STRAPPING Table

## CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal <b>Default</b> 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express <b>Default</b>

 <b>FOXCONN PCEG</b>		
File <b>STRAP</b>		
Size C	Document Number <b>H61MX</b>	Rev A
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**FOXCONN**

**FOXCONN PEG**

File: CPU2-PEG/DMI/FDI

Size: C

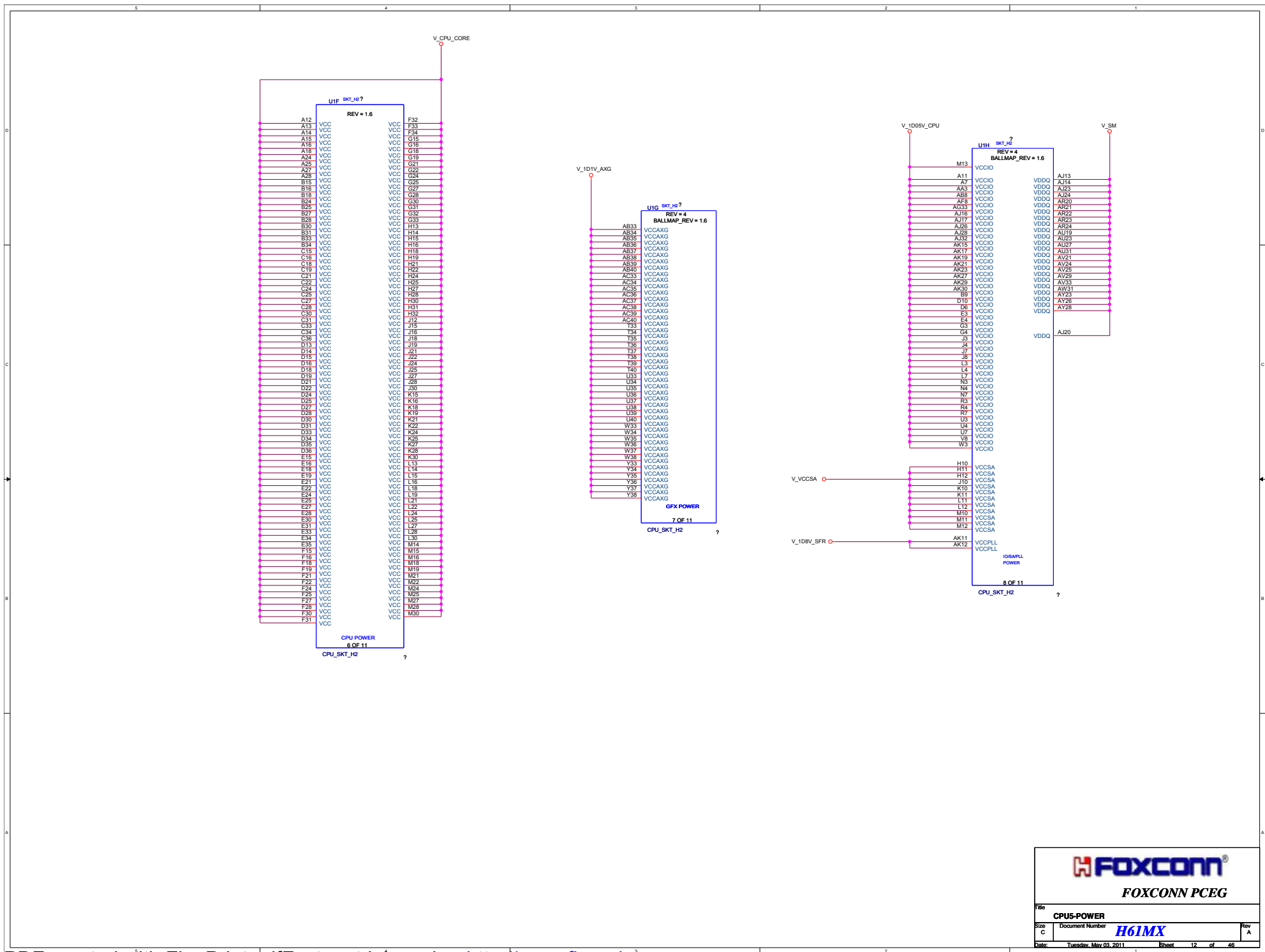
Document Number: H61MX

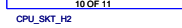
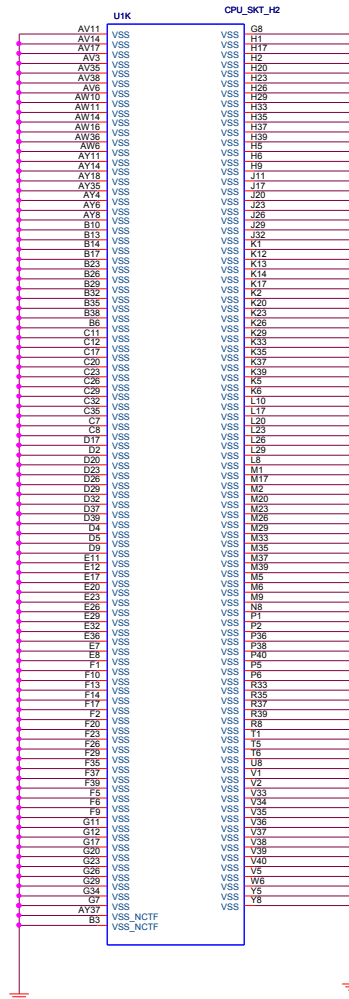
Date: Tuesday, May 03, 2011

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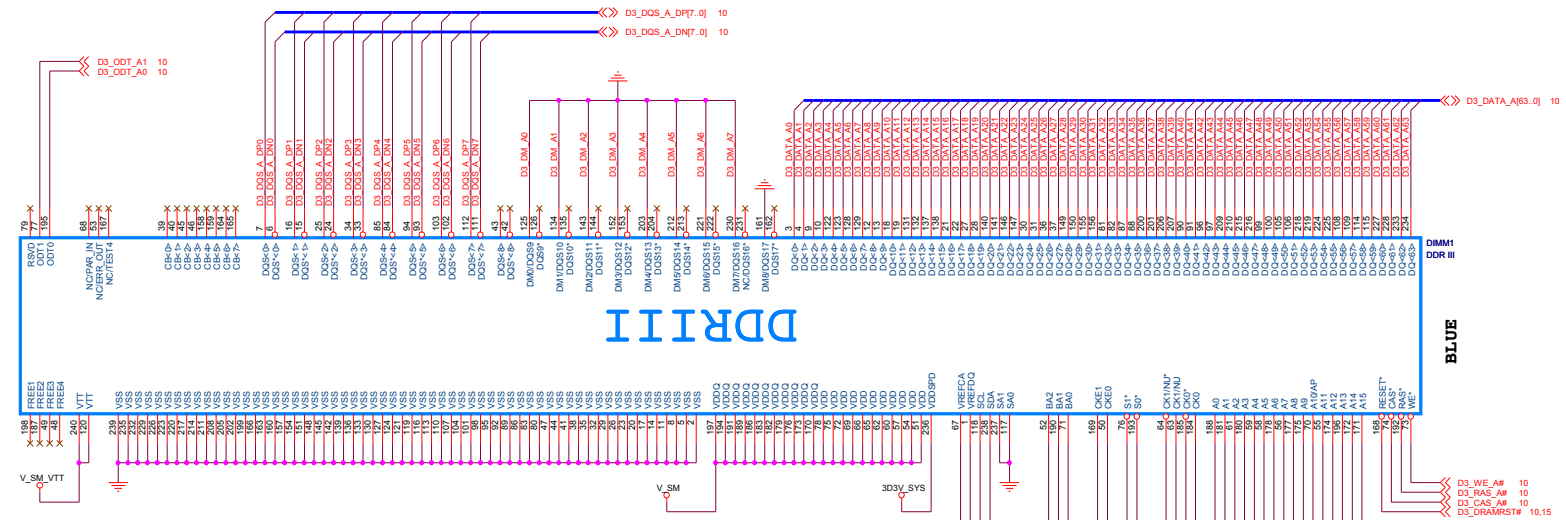




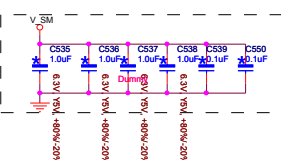




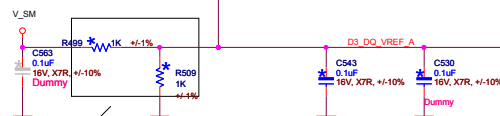
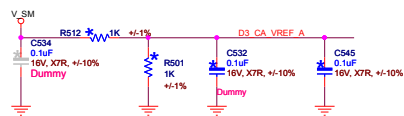
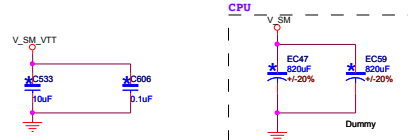
CHANNEL A DIMM 1  
SMB ADDRESS:000



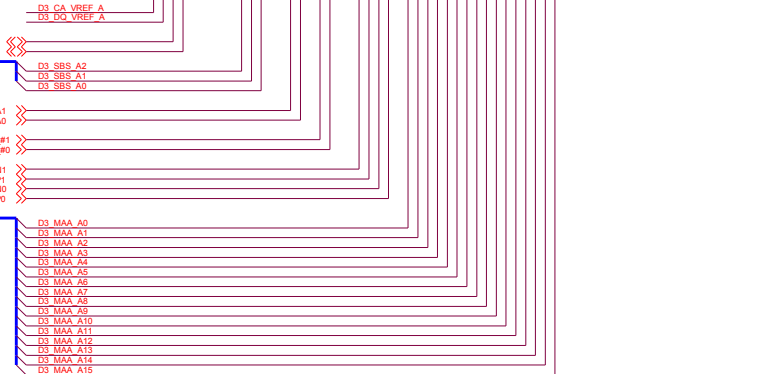
CLOSE TO DIMM POWER PIN



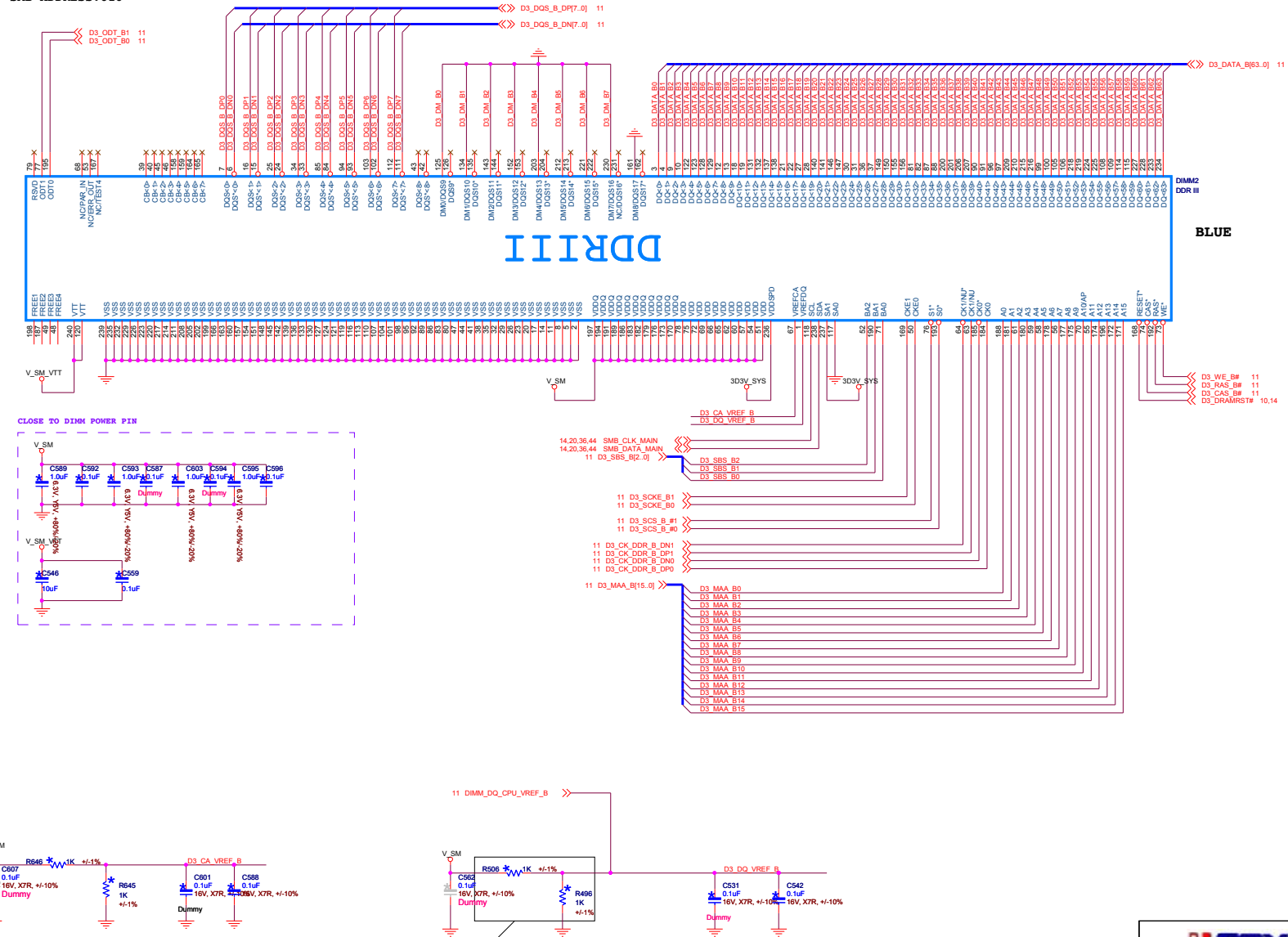
PLACE BETWEEN DIMM1 AND



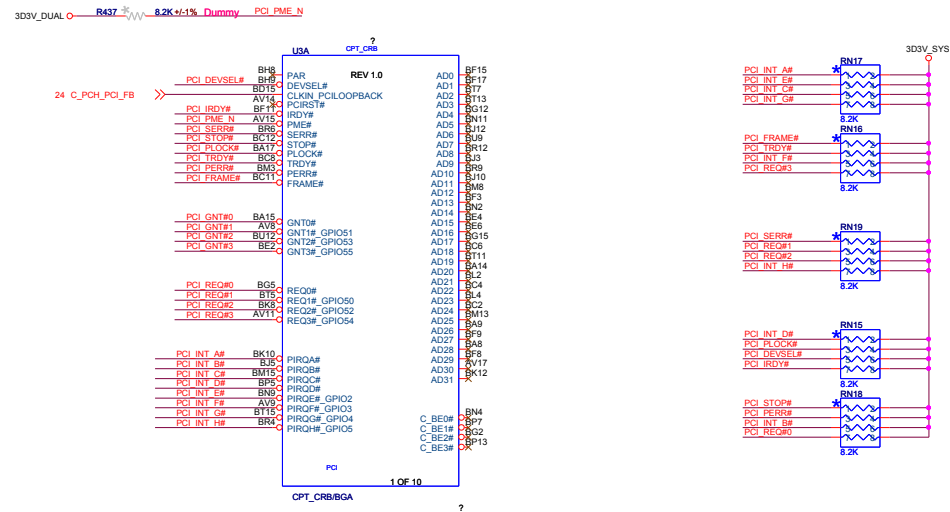
PLACE RESISTORS CLOSE TO CH\_A DIMMS  
ON DIMM\_VREF\_A



Title			
DDR3-1:CHA			
Size	Document Number	Rev	
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STRAP: Boot BIOSselect check whether GNT1 or SATA1GP(GPIO19)

BOOT DEVICE	GNT1	SATA1GP
LPC	0	0
NAND	0	1
PCI	1	0
SPI	1	1

PCI GNT#0 R445 1K Dummy

PCI GNT#1 R438 1K Dummy

Internal pull-up

PCI GNT#3 R446 1K Dummy

PCI GNT#2 R454 1K Dummy

DG 0.7

GNT3 is top block swap mode:  
connect to ground with 4.7k ohm weak  
pull down resistor for top block swap mode

GNT2#/GPIO53:ESI strap for server platform  
ONLY.Do not pull low.



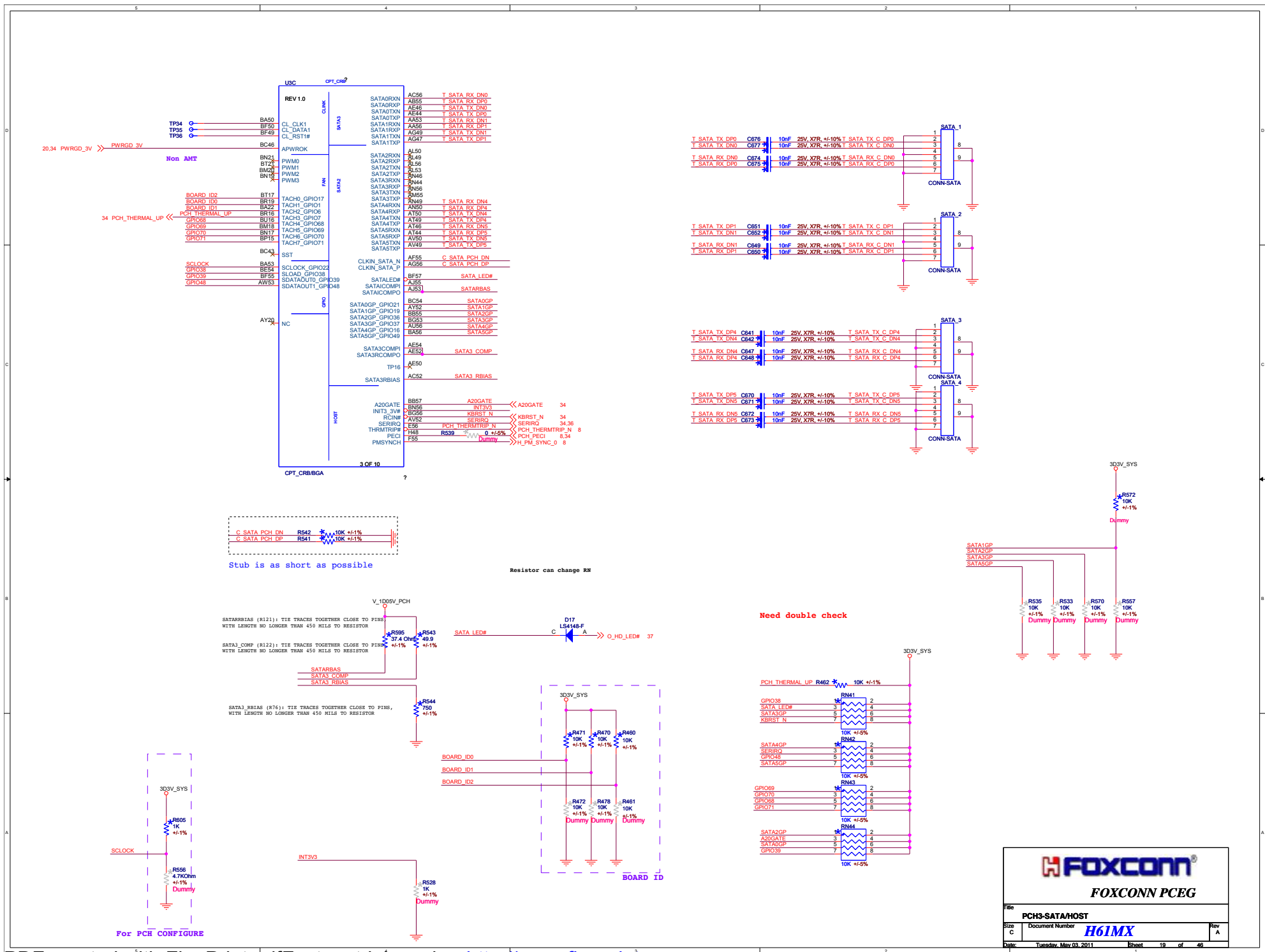
**FOXCONN**  
FOXCONN PCEG

File PCH1-PCI

Size C Document Number H61MX

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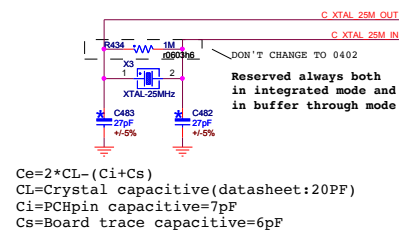
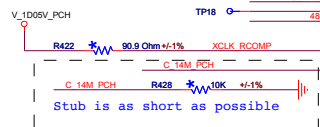
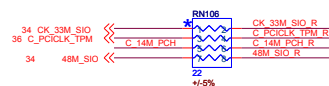
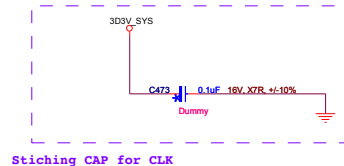




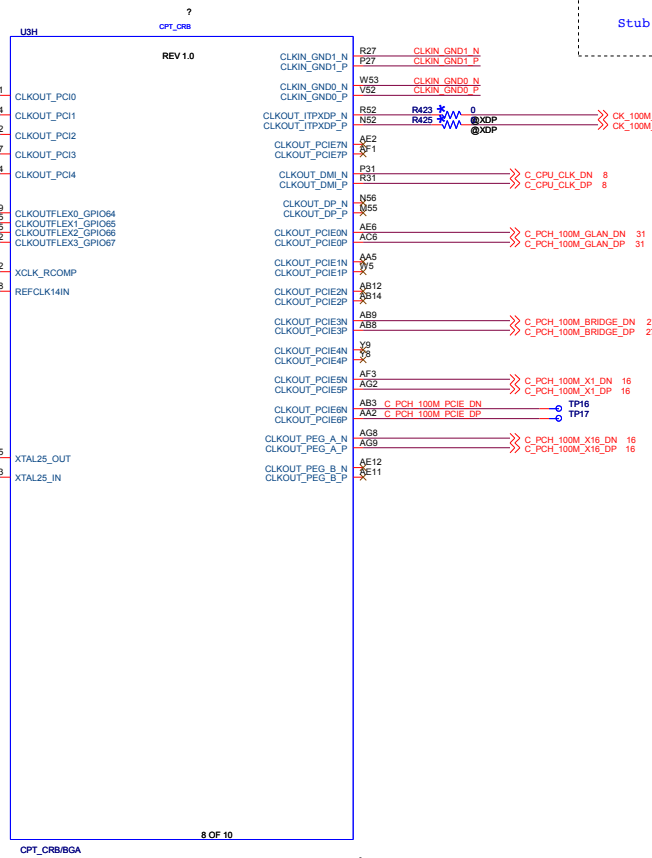
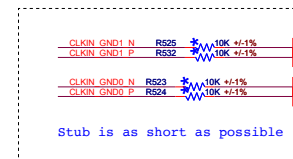






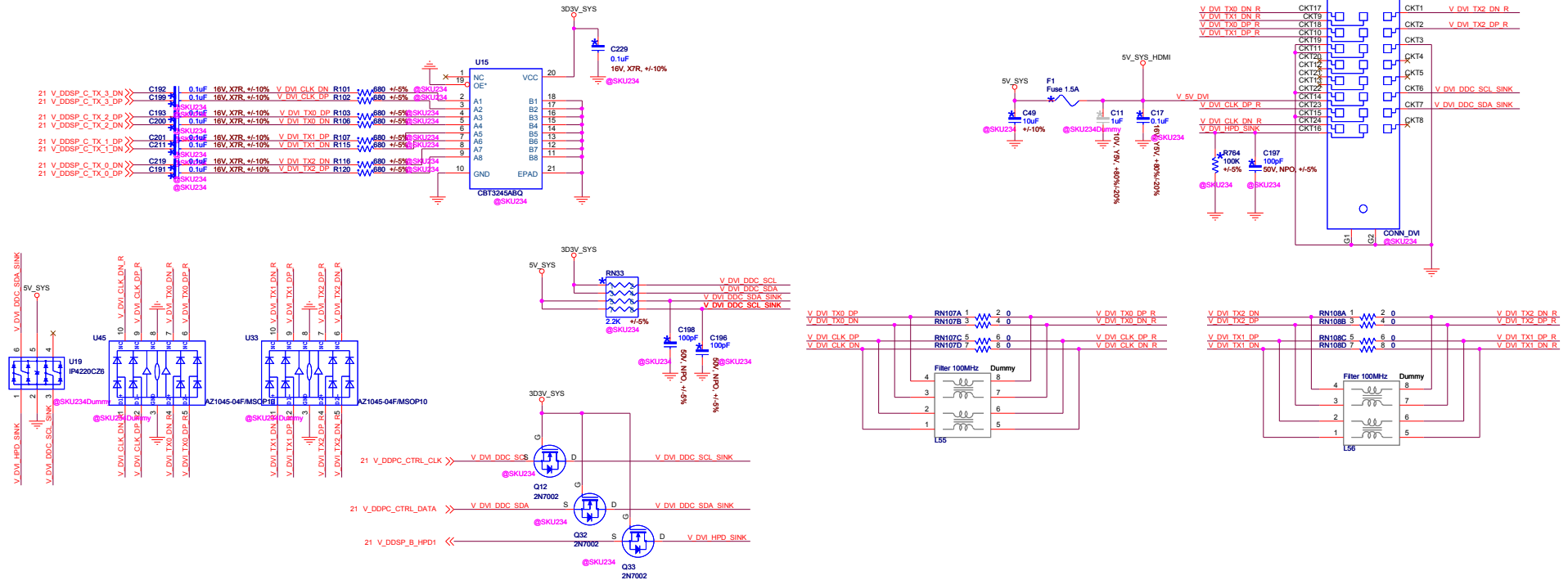


$C_e = 2 * C_L - (C_i + C_s)$   
 $C_L$  = Crystal capacitance (datasheet: 20pF)  
 $C_i$  = PCH pin capacitance = 7pF  
 $C_s$  = Board trace capacitance = 6pF

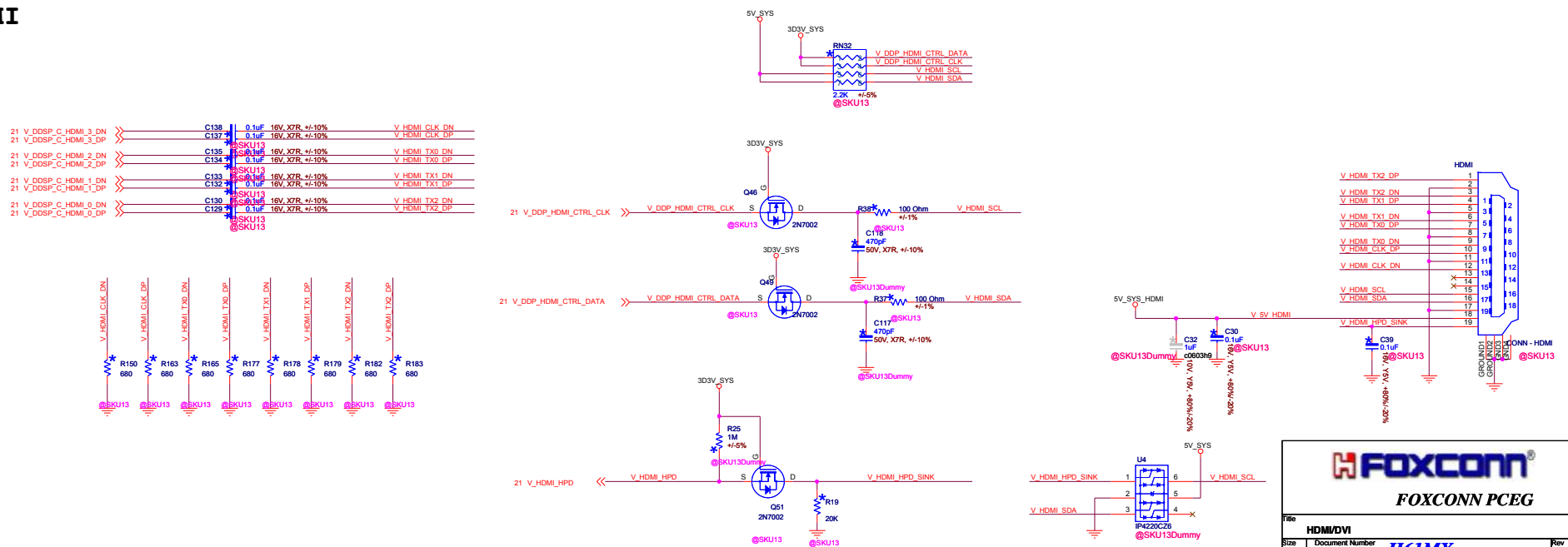




## DVI-D



## HDMI



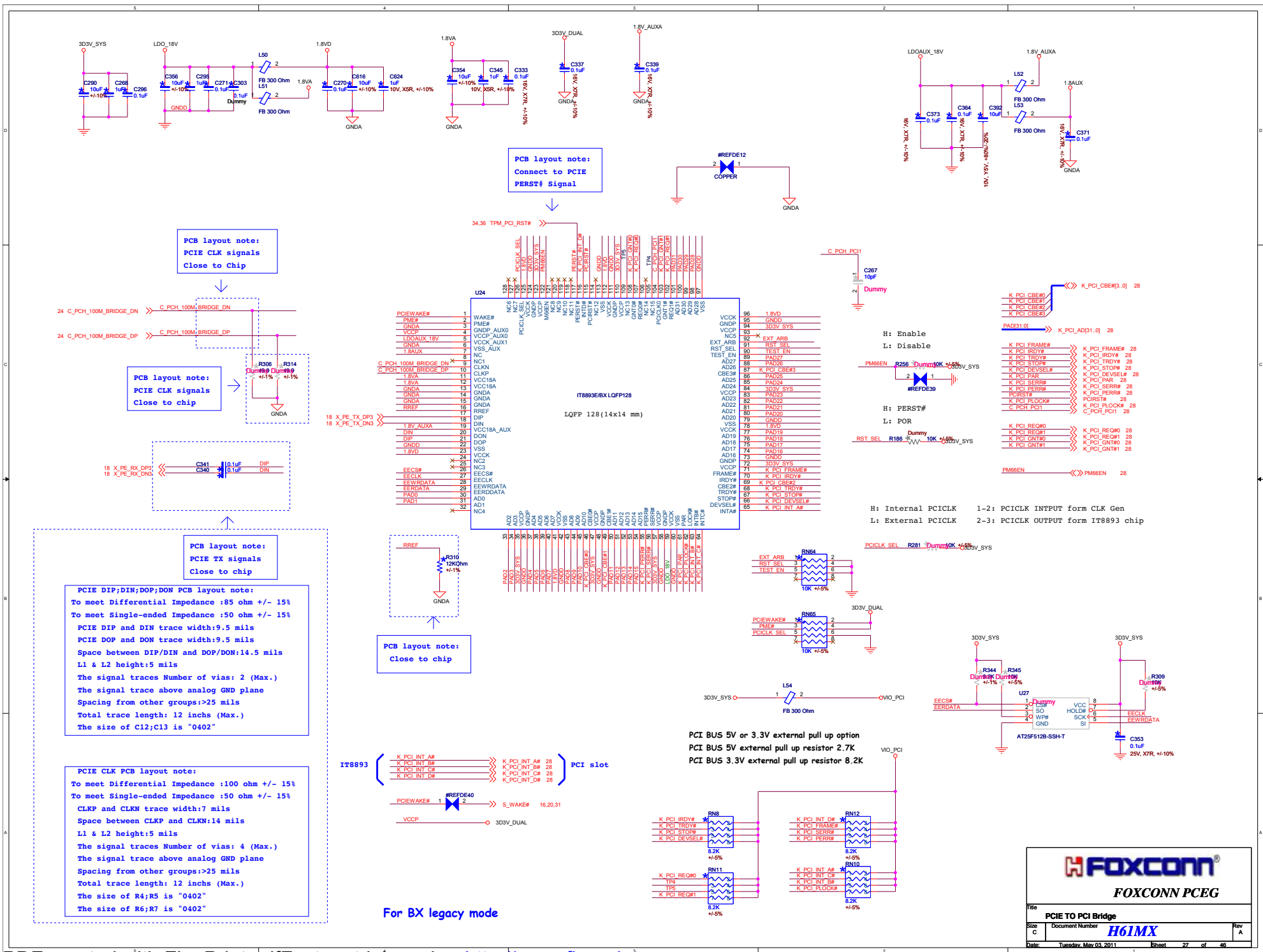
**FOXCONN**

**FOXCONN PCEG**

File: **HDMI/DVI**

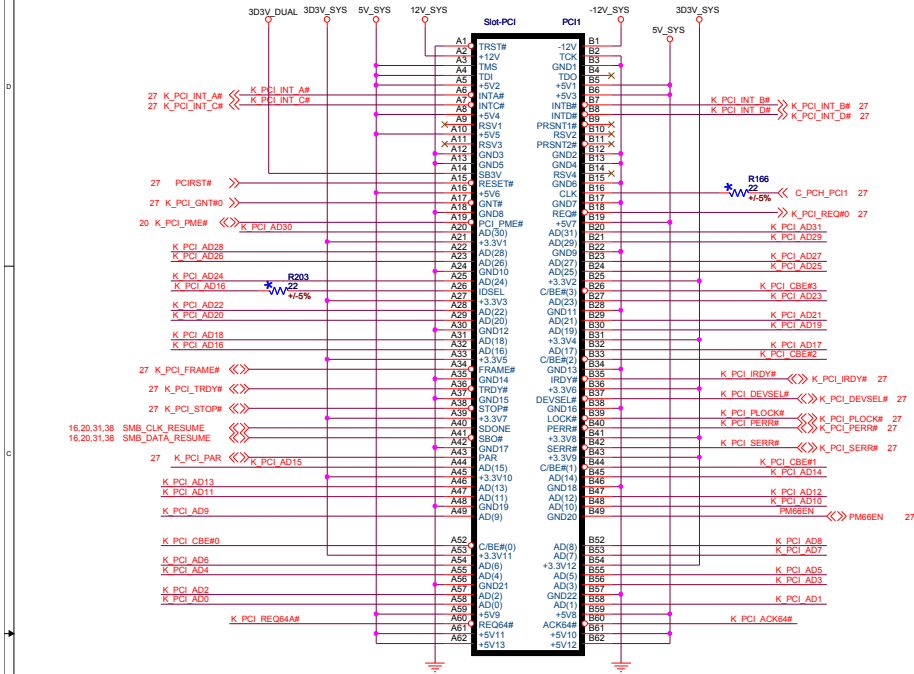
Size: **C** Document Number: **H61MX**

Date: **Tuesday, May 31, 2011** Sheet: **26** of **48**

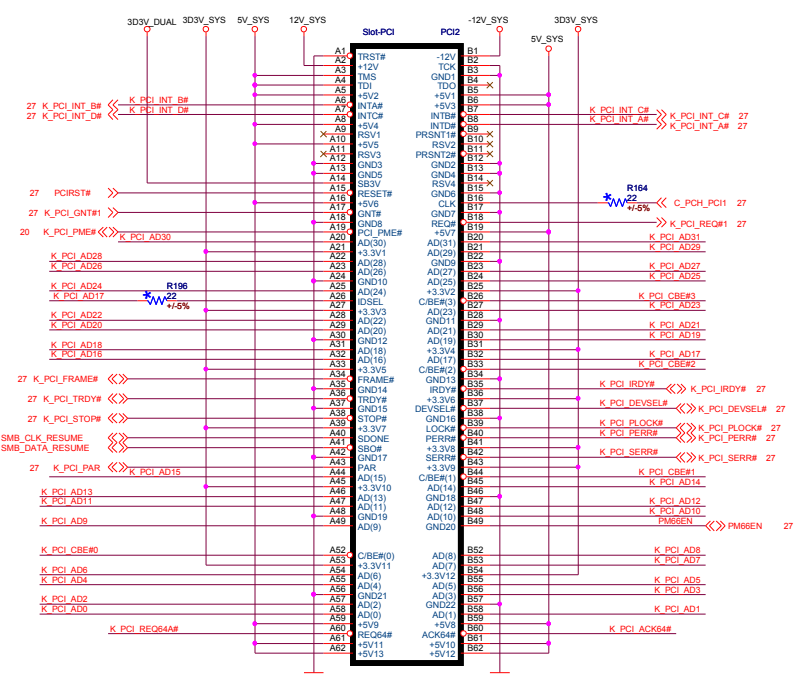


# PCI 1

# PCI 2



IRQ: A B C D  
IDSEL: AD16  
REQ/GNT: 0

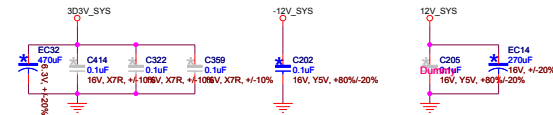
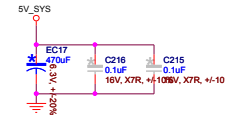


IRQ: B C D A  
IDSEL: AD17  
REQ/GNT: 1

PCI BUS if use 5V external pull up resistor is 2.7K

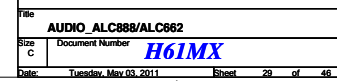
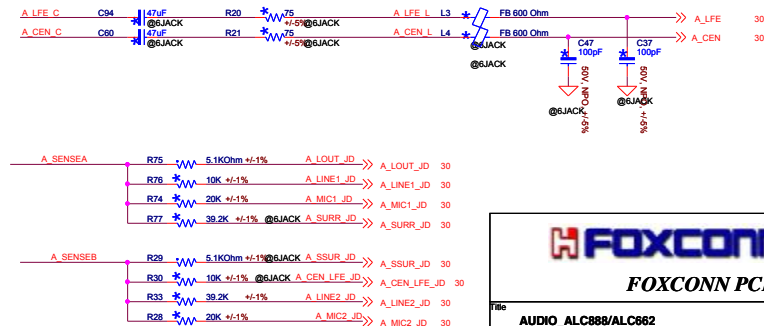
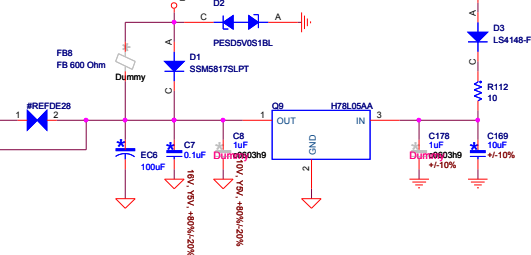
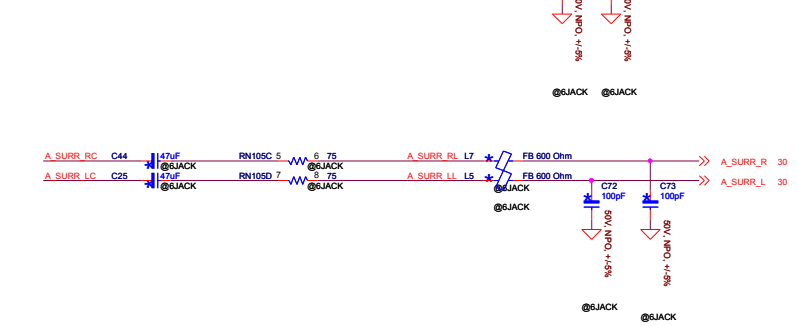
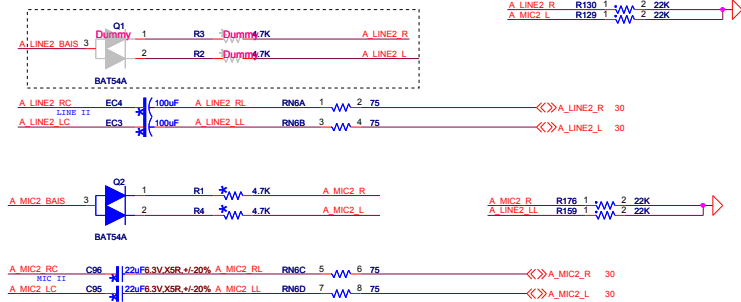
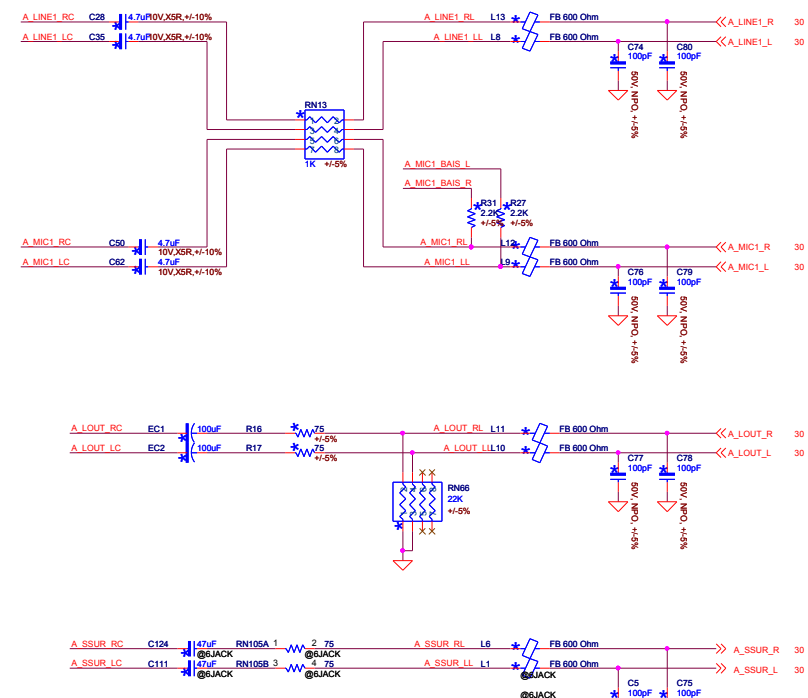


2010.6.22 update

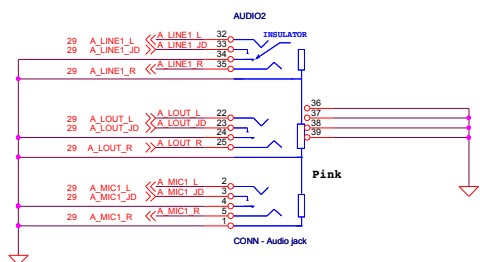
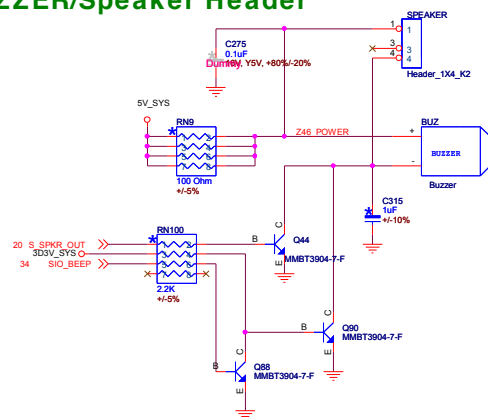


**FOXCONN PCEG**

File	PCI SLOT1/2		
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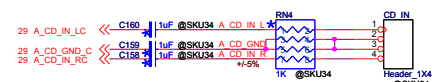
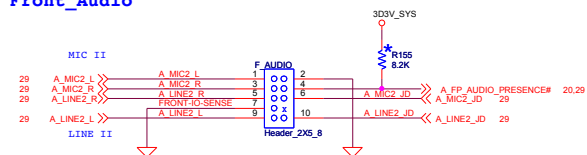
## BUZZER/Speaker Header



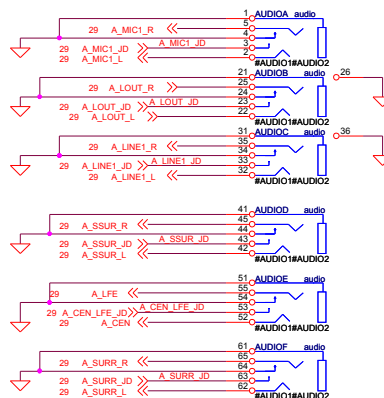
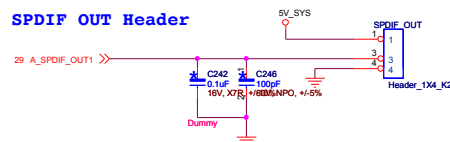
Colay



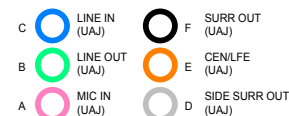
## Front\_Audio



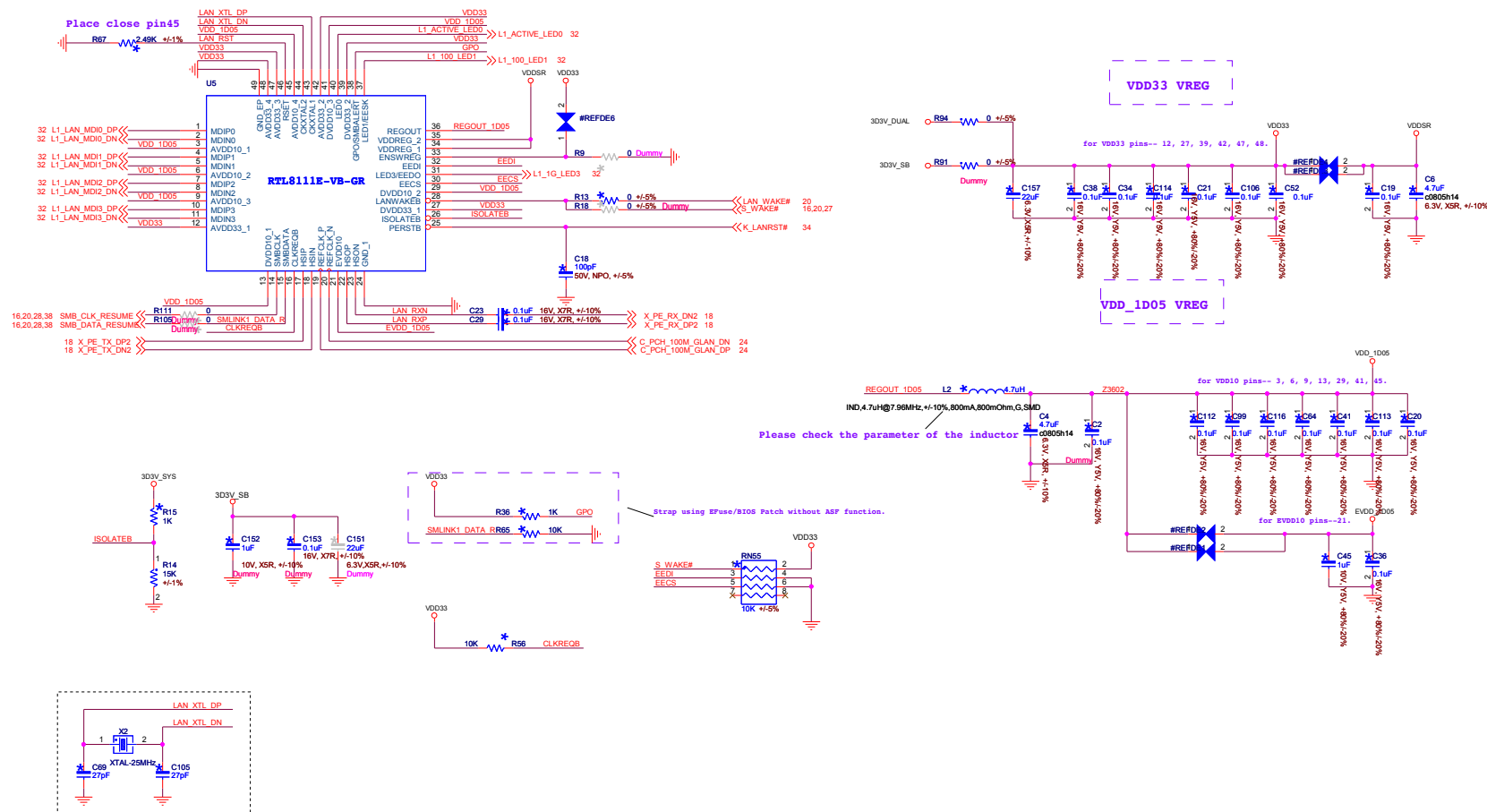
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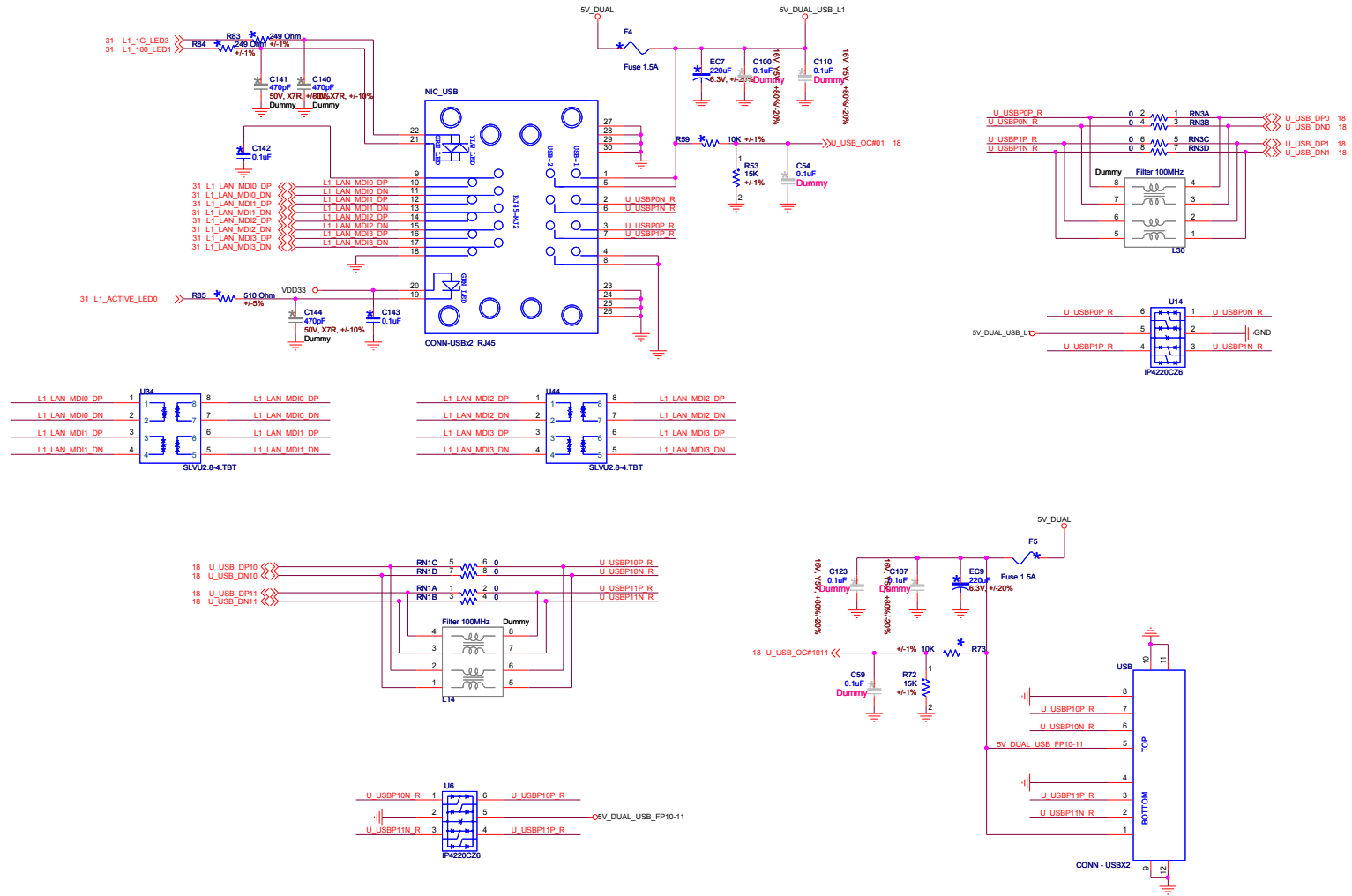


### Audio Jack

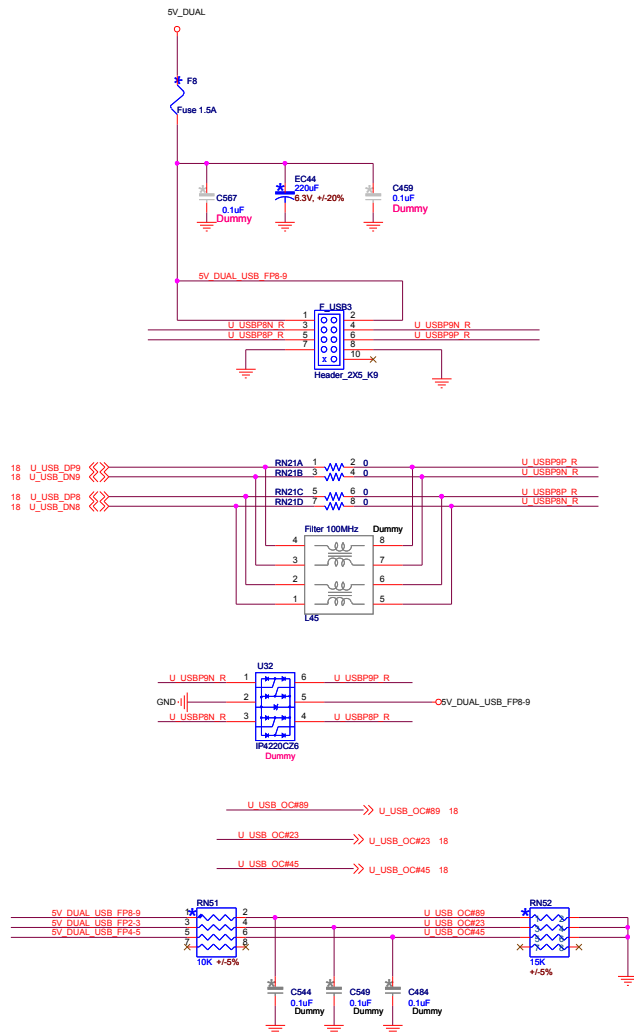


Title		AUDIO CONN/SPDIF/CD-IN	
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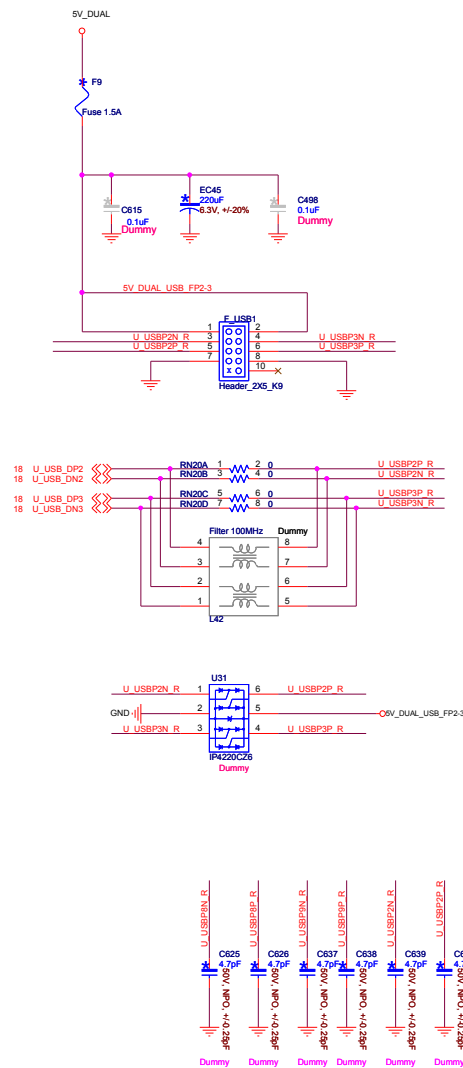




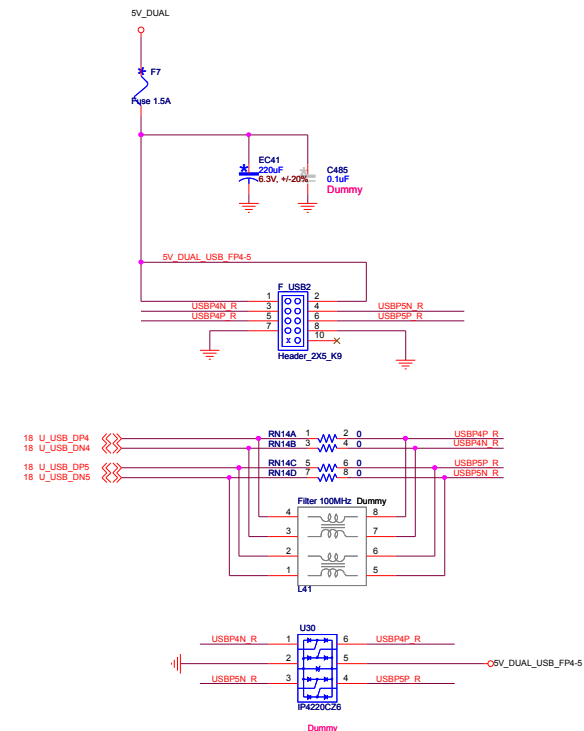
## Front\_USB1



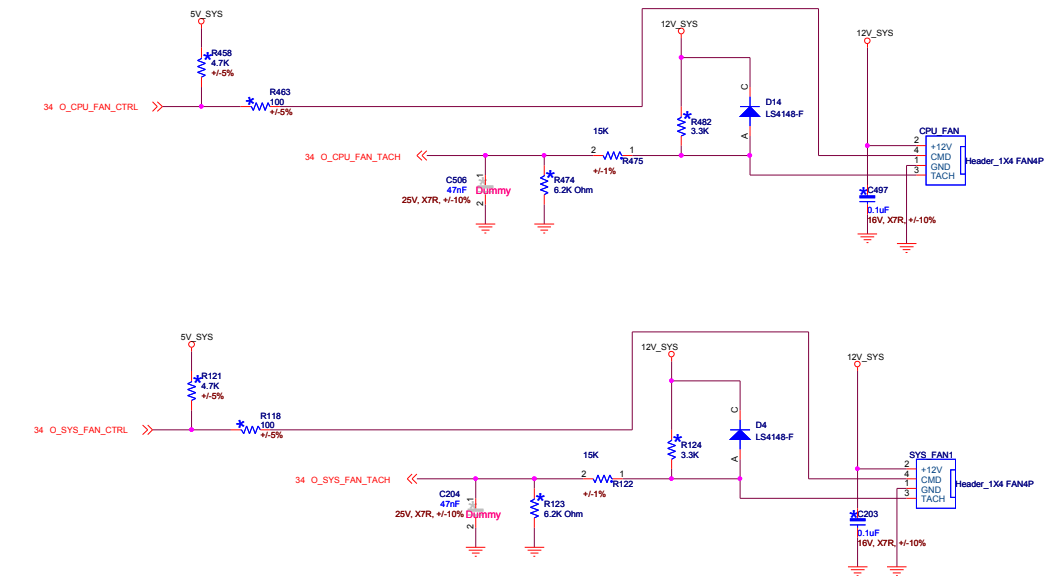
## Front\_USB2



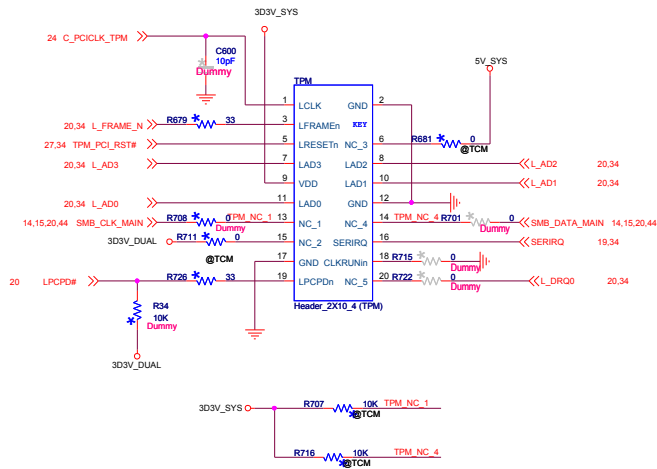
## Front\_USB3



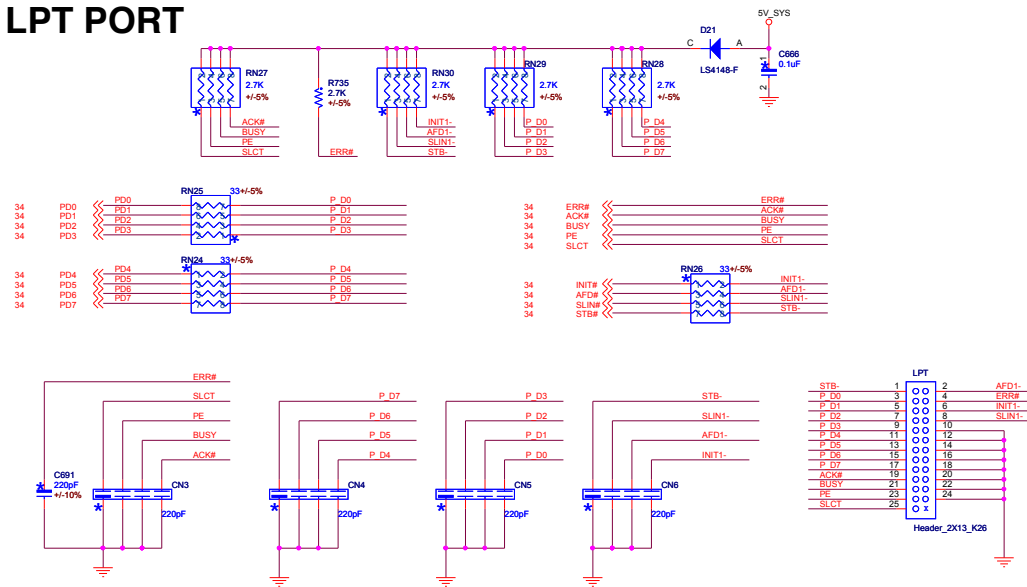




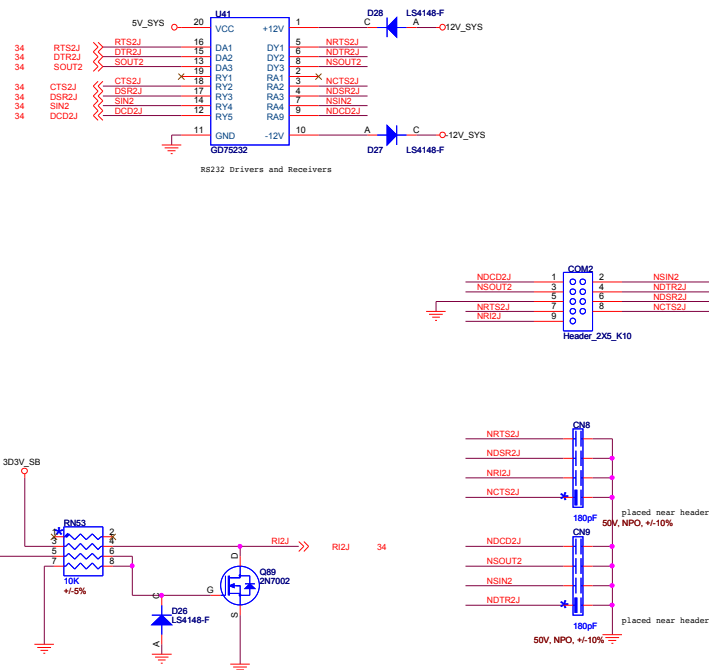
## TPM



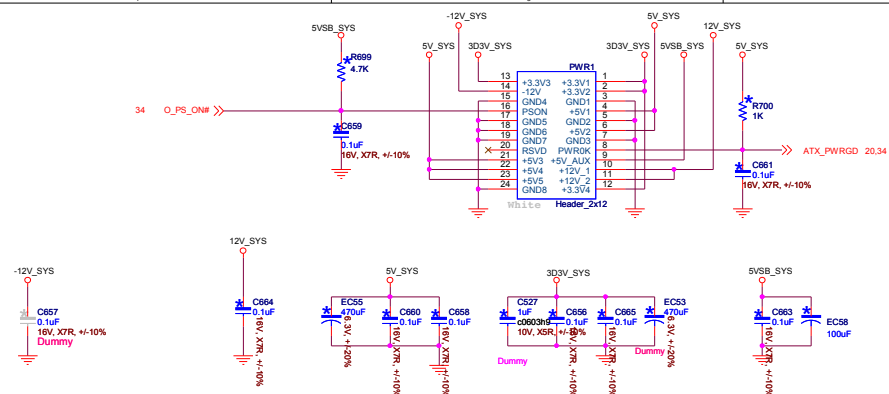
## LPT PORT



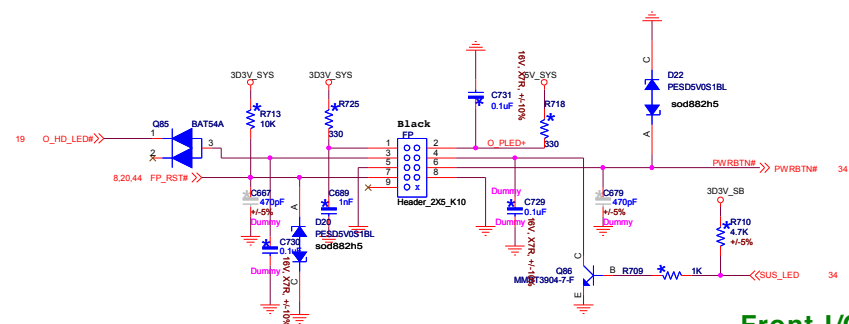
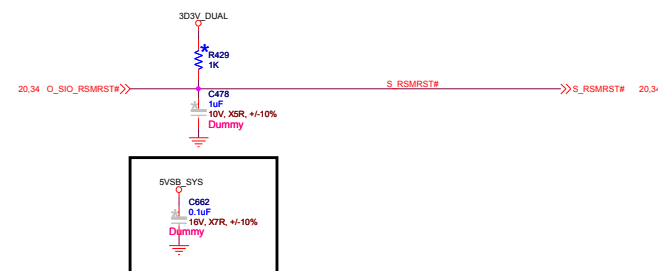
## COM HEADER



## ATX POWER CONNECTOR



## RESUME RESET LOGIC



## Front I/O Header

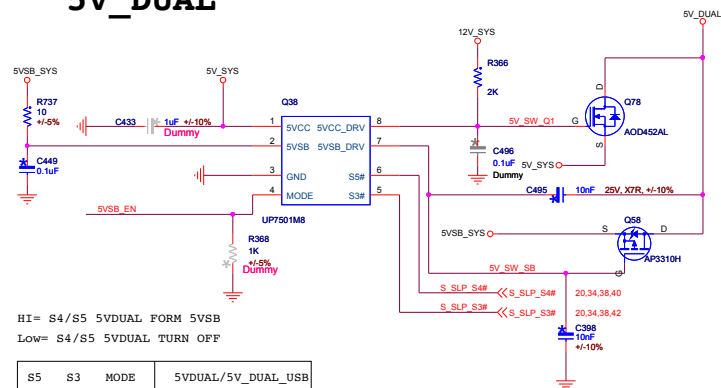
### Front Panel Switch/LED

HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(Green)
GND	5	6	Power button
Reset button	7	8	Detect pin
Detect pin	9	10	Key

S0 : Power LED is on;  
S1 : Power LED is blinking;  
S3~S5: Power LED is off.

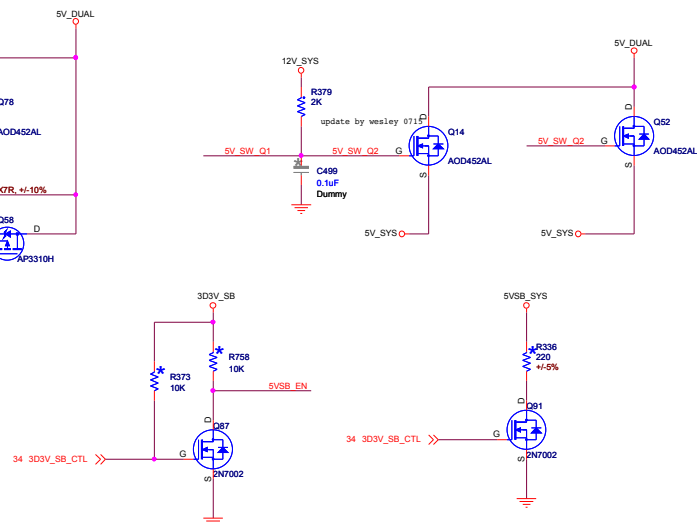


**5V\_DUAL**



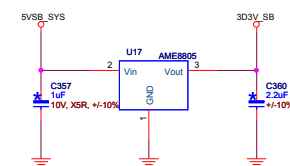
HI= S4/S5 5VDUAL FORM 5VSB  
Low= S4/S5 5VDUAL TURN OFF

S5	S3	MODE	5VDUAL/5V_DUAL_USB
H	H	X	5VCC
H	L	X	5VSB
L	X	H	5VSB
L	X	L	Shutdown

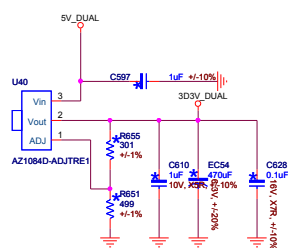


**3D3V\_SB**

Max. output current = 3A

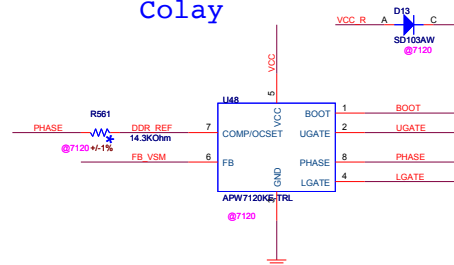


**3D3V\_DUAL**



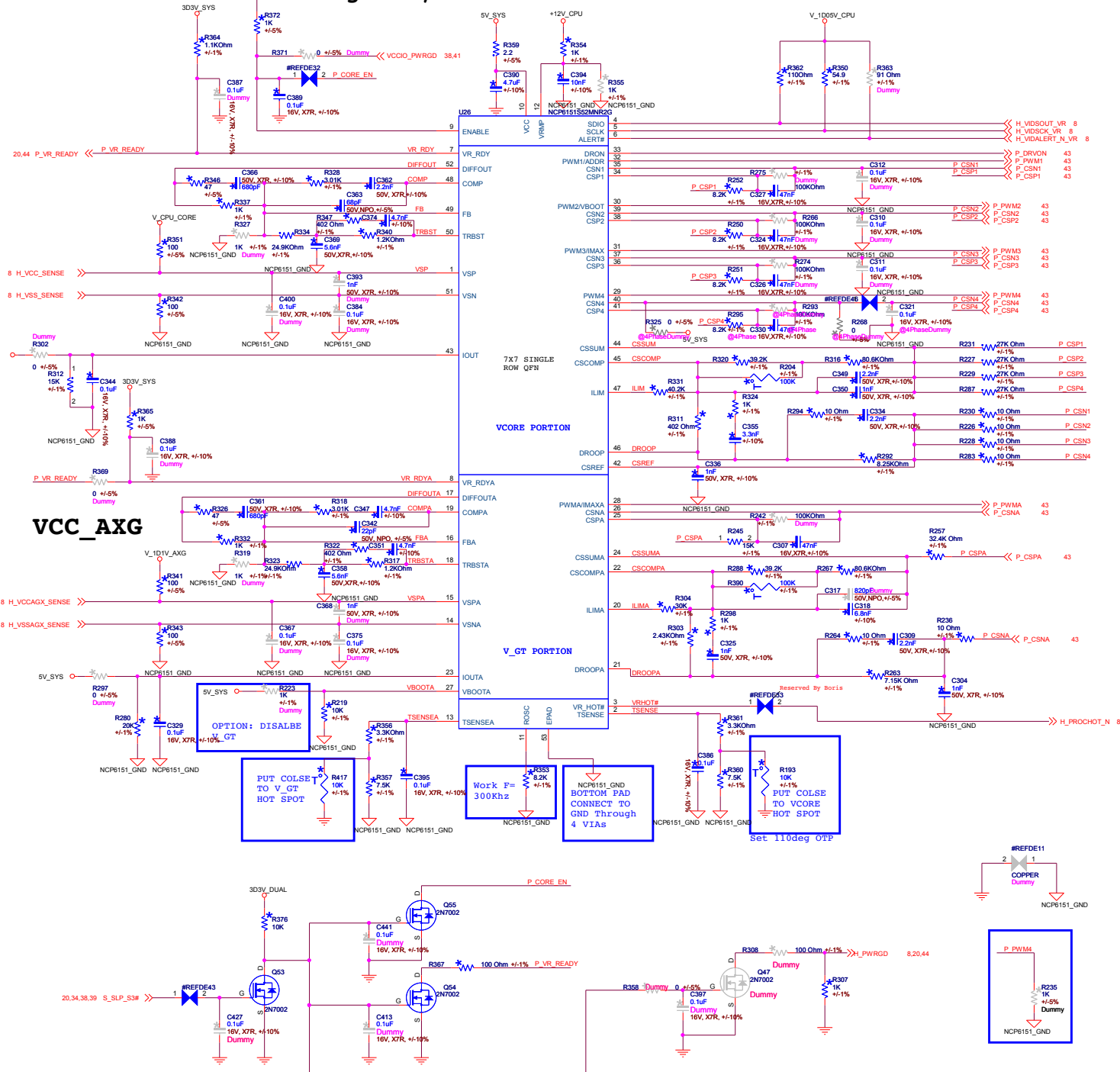
Vout=Vref(1+R2/R1)+IadjR2  
R1 is Up Resistor.  
Iadj=50uA  
Vref=1.25V

Max=40A  
27A in design guide

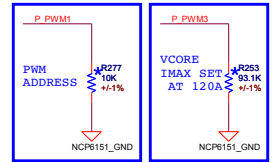
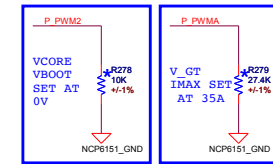




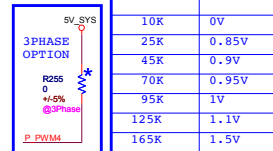
# Sugar Bay VR12 POWER 4+1 PHASE



## VCC\_CORE



## BOOT VOLTAGE



## PWM ADDRESS

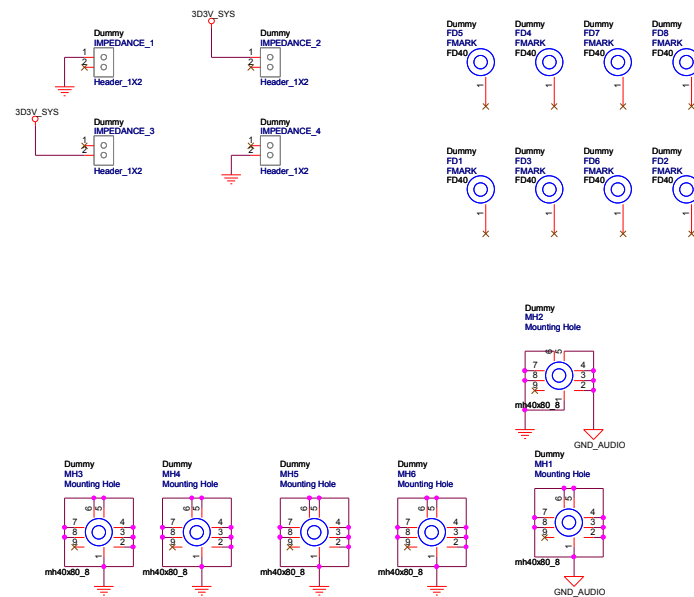
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

**FOXCONN**  
FOXCONN PCEG

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 <p><b>FOXCONN PCEG</b></p>			
File <b>Changelist</b>			
Size	Document Number	<b>H61MX</b>	Rev
C			A
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